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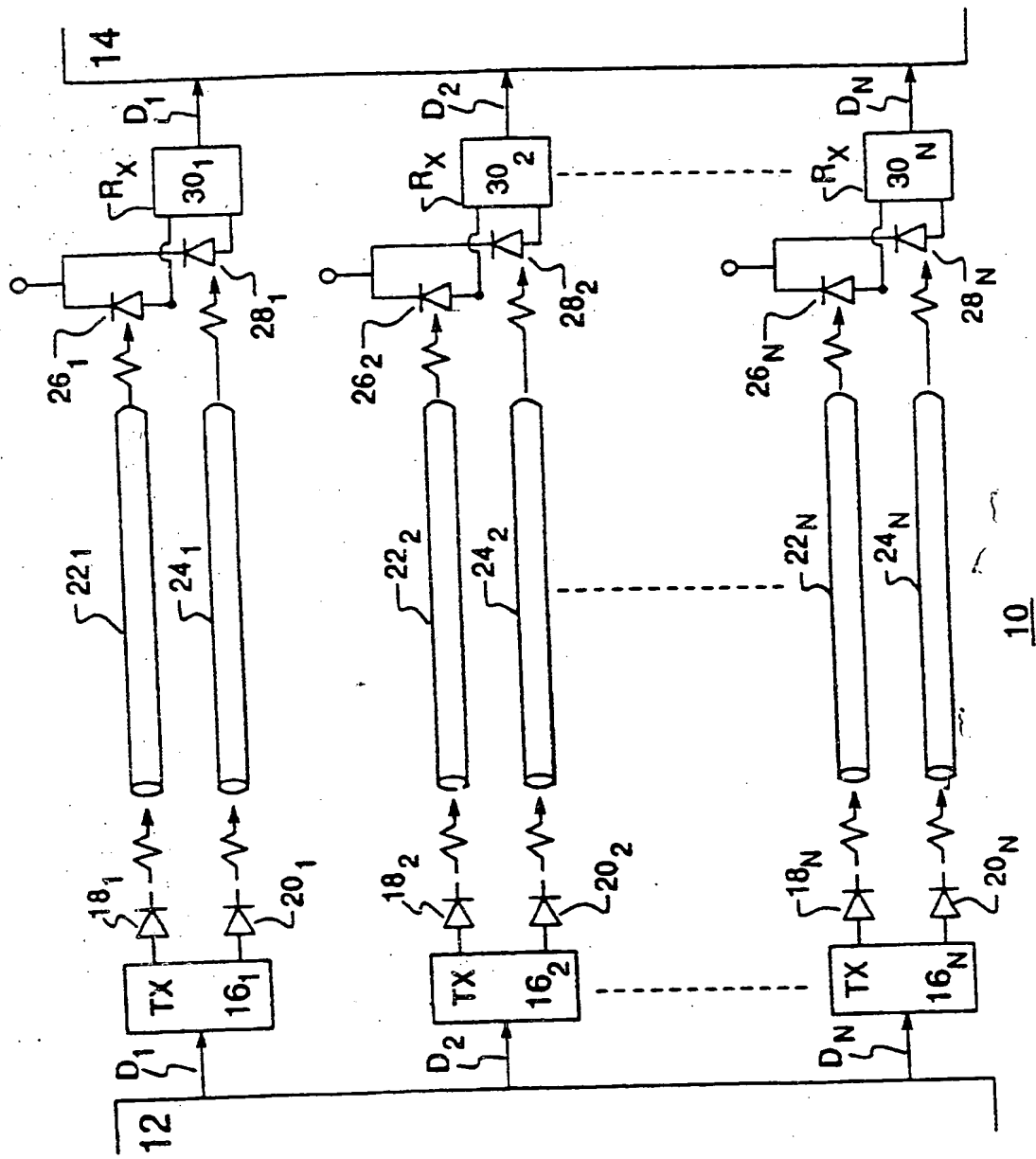
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(54) **Dc-coupled optical data link utilizing differential transmission.**

(57) A data link (10) is disclosed which utilizes differential communication between pairs of transmitting (18,20) and receiving (26,28) devices. In particular, one device (18) of each pair is reserved for communicating a logic "0" and the other (20) is reserved for communicating a logic "1". The pairs are grouped to form an array which is capable of providing simultaneous parallel communication, at relatively low bit rates, between two equipment components (12,14). The communication may be either unidirectional or bidirectional between the components. The ability to integrate the arrays of transmitting and/or receiving electronics and optics allows for improved reliability of the system over a single fiber, high data rate, alternative.

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FIG. 1



Background of the Invention

Field of the Invention

The present invention relates to a DC-coupled optical data link utilizing differential transmission and, more particularly, to a system which utilizes an array of paired transmitting devices and an array of paired receiving devices to achieve communication, with one device of each pair dedicated to transmission of a logic "0" and the other dedicated to transmission of a logic "1".

Description of the Prior Art

There is a growing need to be able to optically interconnect backplanes of computers and communication equipment over relatively short distances (10-100 meters, for example). Current applications consist primarily of massive parallel data interfaces (typically 32-64 lines) with parallel clocking rates (typically 20-50 MHz). The aggregate data bandwidth, therefore, is within the range of 0.5-4.0 Gb/s. Although there exist many optical systems which are capable of handling this bandwidth with a single fiber interconnection, the cost, size, complexity and power requirements of such interconnections are considered to be overwhelming for many low cost applications.

Summary of the Invention

The need remaining in the prior art is addressed by the present invention which relates to a DC-coupled optical data link utilizing differential transmission and, more particularly, to a system which utilizes an array of paired transmitting devices and an array of paired receiving devices, coupled together by an array of paired optical signal paths, to provide transmission suitable for optical backplane applications.

In accordance with one embodiment of the present invention, a pair of transmitting devices are used to transmit a given data stream, with the first device being activated to transmit a logic "1" and the second device being activated to transmit a logic "0". Similarly, a pair of receiving devices are used to recover the data stream, where the data is recovered by comparing the photocurrent outputs from the pair of devices. Advantageously, an array of 2N transmitting devices, coupled in pairs to a set of data inputs may be used to form a set of N data channels for simultaneously transmitting N separate data streams. It is to be understood that individual data signals may be multiplexed together to form a single data stream so that the array system of the present invention is actually capable of transmitting MxN signals, where M is number of data signals/stream.

In another embodiment of the present invention, bidirectional communication is achieved by utilizing

the semiconductor devices at each end of the data channel as both transmit and receive devices. Accordingly, transmit and receive circuitry is then located at each end of the channel.

Further, amplification of the transmitted signal may be obtained, in another embodiment of the present invention, by using a laser gain medium, for example, a laser amplifier, coupled to each pair of waveguides. Since the gain medium will preferentially amplify the transmitted data signal with respect to any background noise present along the inactive waveguide, the amplifier also serves as a filter to the communication system.

An advantage of the present invention is that by utilizing pairs of transmitters, optical paths and receivers to transmit data, the relative DC level of the pair of signals is unchanging (i.e., fixed at zero), allowing relatively simple emitter-coupled logic (ECL) transmitter and receiver circuits to be used.

An additional advantage may be realized in one embodiment of the present invention where integrated arrays of transmitter and receiver optical devices are used. Integration provides for inherent matching of components, resulting in substantially equal power being emitted from the transmitting devices, and substantially equal photocurrents being developed by the receiving devices. The use of integrated arrays will provide further advantages to the system in terms of inter-device tracking as a function of, for example, temperature, age or alignment. The match inherent in optical devices allows for further simplification in the electronic circuitry.

For one particular embodiment of the present invention, the need to provide special signal encoding for the purposes of clock recovery may be eliminated by reserving one pair of lines for transmission of a system clock. Therefore, for a conventional fiber ribbon cable of twelve (or eighteen) individual fibers, one clock signal and five (or eight) data streams (each stream having one or more separate data signals) may be simultaneously transmitted.

Other and further advantages of the present invention will become apparent during the course of the following discussion and by reference to the accompanying drawings.

Brief Description of the Drawing

Referring now to the drawings, where like numerals represent like parts in several views:

FIG. 1 illustrates an exemplary differential array optical data link formed in accordance with the present invention;

FIG. 2 illustrates an alternative differential array optical data link capable of providing bidirectional transmission in accordance with the present invention;

FIG. 3 illustrates yet another bidirectional array

optical data link, utilizing same semiconductor optical devices for both transmission and reception;

FIG. 4 contains a graph illustrating the presence of pulse width distortion in conventional optical transmissions;

FIG. 5 contains a graph illustrating the elimination of pulse width distortion in the differential signaling scheme of the present invention;

FIG. 6 illustrates an exemplary ECL transmitter which may be used in the system of the present invention; and

FIG. 7 illustrates an exemplary ECL receiver which may be used in the system of the present invention.

Detailed Description

An exemplary differential array optical data link 10 of the present invention is illustrated in FIG. 1. As discussed above and shown in FIG. 1, such a data link may advantageously be utilized as an optical back-plane interconnect between a first equipment component 12 (for example, a personal computer) and a second equipment component 14 (for example, a mass storage device or cache memory device). In accordance with the present invention, each data channel is associated with two distinguishable (e.g., separate polarizations or separate fibers) optical signal paths, one path for transmitting a logic "0" and the other for transmitting a logic "1". For the remainder of the present discussion, the optical signal path will be discussed in terms of an optical fiber. However, it is to be understood that the present invention is not limited to utilizing optical fibers as the optical transmission media.

Referring to FIG. 1, a first data stream D_1 is applied as an input to a first transmitter 16_1 , the output of transmitter 16_1 being coupled to a pair of light emitting devices $18_1, 20_1$, where devices $18_1, 20_1$ may be lasers or LEDs. An exemplary transmitter 16_1 will be discussed in detail below in association with FIG. 6. In general, transmitter 16_1 is configured to activate device 18_1 to transmit a logic "0" and activate device 20_1 to transmit a logic "1". As shown device 18_1 is coupled to the near end of optical fiber 22_1 and device 20_1 is coupled to the near end of fiber 24_1 . The far ends of fibers 22_1 and 24_1 are coupled to a pair of optical devices 26_1 and 28_1 , respectively, where devices $26_1, 28_1$ may comprise PIN or avalanche photodiodes, or any other suitable optical receiving devices. The electrical output signals from devices $26_1, 28_1$ are applied as inputs to a receiver 30_1 which recovers the transmitted data stream D_1 . Receiving devices $26_1, 28_1$ may be considered as forming part of a receiver circuit 30_1 , where an exemplary receiver 30_1 will be discussed in detail below in association with FIG. 7.

As discussed above, the system of the present invention is particularly advantageous for array applications with multiple LED (or laser) and PIN arrays (or alternatively, arrays of other transmitting and/or receiving devices). Referring to FIG. 1, additional data streams D_2, \dots, D_N are illustrated as applied to the inputs of transmitters $16_2, \dots, 16_N$. Devices $18_2, 20_2$ through $18_N, 20_N$ are then activated in accordance with the data streams and the light outputs are propagated along fibers $22_2, 24_2$ through $22_N, 24_N$ to receivers $30_2 - 30_N$. In association with such an array application, there exist many techniques for forming large arrays of semiconductor optical devices on a single substrate. For example, an article entitled "GaInAsP distributed feedback laser array" by Y. Twu et al. appearing in *Electronic Letters*, Vol. 24, No. 2, June 1988 at pp. 743-4 discusses a particular fabrication technique suitable for laser array applications. Fabrication techniques for LED and PIN arrays are described in an article entitled "12-channel Ph and LED arrays and their packaging for $1.3 \mu m$ applications", by Y. Ota et al., appearing in *Proceedings SPIE*, Vol. 839, 1988 at pp. 143-7. Since a monolithic array of optical devices will have been subject to identical processing sequences, the devices will contain essentially identical performance characteristics (in terms of temperature tracking, aging, alignment, etc.).

For embodiments utilizing fiber as the interconnecting signal paths, the preferred embodiment with present technology would consist of a conventional twelve (or eighteen) fiber ribbon cable. Therefore, the embodiment would include a set of six (or nine) physical data channels. By using various multiplexing schemes, the number of data signals transmitted over each channel may be increased. In this case, the transmission of a frame clock becomes a requirement and one of the six (nine) channels may be reserved for this purpose. Thus, the five (eight) remaining data channels may be multiplexed to carry M separate separate data signals (where M may vary from channel to channel).

A differential data link of the present invention may also be configured as a bidirectional communication system. An exemplary bidirectional differential data link 100 is illustrated in FIG. 2. Similar to the arrangement of FIG. 1, link 100 is utilized to provide communication between first equipment component 12 and second equipment component 14 over a plurality of N data channels, each channel comprising a pair of optical fibers $22_i, 24_i$. For the sake of clarity, only the " i th" channel is illustrated in FIG. 2. It is to be understood that in implementation, bidirectional data link 10, like data link 10 of FIG. 1, comprises a plurality of N data channels, each constructed in a manner similar to that shown in FIG. 2. In accordance with the present invention, bidirectional communication is achieved by including optical transmitting and receiving devices with both components 12 and 14. In par-

ticular, a second pair of transmitting devices 18_i, 20_i are co-located with receiving devices 26_i, 28_i at component 14. Similarly, a second pair of receiving devices 26_i, 28_i are co-located with transmitting devices 18_i, 20_i at component 12.

In operation of bidirectional data link 100, communication from equipment component 12 to equipment component 14 occurs as discussed above with the embodiment of FIG. 1. In the reverse direction, a data signal D_i from equipment component 14 is applied as an input to differential transmitter circuit 16_i. The pair of outputs from circuit 16_i are then applied as inputs to transmitting devices 18_i, 20_i for propagation over the "ith" communication channel (via fibers 22_i, 24_i) to equipment component 12. At component 12, the received signal is coupled to the pair of receiving devices 26_i, 30_i for conversion into an electrical signal. The pair of electrical outputs are then applied as inputs to differential receiver circuit 30_i to recover the transmitted data signal D_i, which is subsequently applied as an input to equipment component 12. In order to accomplish the actual coupling of the optical signals to the optical devices, it is seen that fiber 22_i is modified to include a first splitter 102 at component 12 and a second splitter 104 at component 14. Similarly, fiber 24_i is modified to include a first splitter 106 at component 12 and a second splitter 108 at component 14. In particular, splitter 102 couples transmitting device 18_i and receiving device 26_i to fiber 22_i, and splitter 104 couples receiving device 26_i and transmitting device 18_i to fiber 22_i. Splitters 106, 108 provide a similar function with respect to devices 20_i, 28_i, 28_i, 20_i and fiber 24_i.

As shown, the arrangement of FIG. 2 is capable of providing full duplex, bidirectional communication between equipment components 12 and 14. In certain circumstances, it may be desirable to reduce the number of active devices associated with either equipment component, while still providing bidirectional communication. In this case, a half duplex arrangement 120, as illustrated in FIG. 3, may be the preferred alternative. In this particular embodiment, the same pair of devices, for example, devices 18_i, 20_i at the near end and 26_i, 28_i at the far end, are used as both transmitting and receiving devices. It is well-known in the art that an LED may behave as either a light emitter or light receptor, depending upon the bias applied thereto. Thus, arrays of LEDs may be used in this particular embodiment to provide bidirectional communication. As with the arrangement of FIG. 2, additional circuitry is required to effect bidirectional communication. In particular, a transmitter circuit 16_i is co-located with receiver circuit 30_i at component 14 to provide the return data signal D_i to devices 26_i, 28_i. Similarly, a receiver circuit 30_i is co-located with transmitter circuit 16_i at component 12 to receive electrical output from devices 18_i, 20_i and enable recovery of the transmitted return signal D_i. Advantageously,

the co-located transmitter and receiver circuitry may be integrated on a single substrate to decrease the overall size of the data link.

For the particular embodiment 120 of FIG. 3, it becomes important to provide a means for controlling the direction of signal flow during a given period of time. One method of providing this control is to dedicate one channel to the transmission of a system clock. A system clock would allow, for example, component 12 to transmit during only a first designated time period τ_1 , and component 14 to transmit during only a second designated time period τ_2 . It is to be understood that there exist many other means of controlling the communication of information between the two equipment components 12 and 14.

An advantage of the present invention is the use of differential transmission in the form of a pair of paths used to form a single data channel. Differential transmission allows for the receiver circuitry to be formed with differential logic, with the threshold level set at zero. Simply, a receiver 30_i (30_i) merely compares the photocurrent outputs from devices 26_i, 28_i (18_i, 20_i) and forms the recovered data signal by determining which device produces the largest signal. In particular, if the output from device 26_i (18_i) is greater, the recovered bit is defined as a logic "0". Alternatively, if the output from device 28_i (20_i) is greater, the recovered bit is defined as a logic "1".

The use of such a differential recovery arrangement allows the inventive system to be essentially immune to pulse width distortion at the receiver input. Pulse width distortion is a problem in conventional systems which use a single fiber to transmit both logic signals. FIG. 4 is illustrative of the pulse width distortion problem. In a conventional receiver, a fixed threshold DC level TH is used to determine which logic bit has been received. FIG. 4 illustrates three different signal power levels, indicated by the appropriate letters L (low), S (standard) and H (high). For low received signal power, various factors, including RC time constants related to the receiver electronics, fiber dispersion, and transmitter rise/fall times, result in the transition from logic "0" to logic "1" to occur at point A, and the transition back to logic "0" at point B. The resultant output pulse from the receiver is also illustrated. For standard signal levels, the transitions are seen to occur at points C and D, and the output pulse is of the shape illustrated below the received signals. When the receiver is overdriven and the signal power exceeds the specified value, the transitions are shown to occur at points E and F, with the resulting output data signal as shown. Clearly, pulse width distortion will be present in this system, as indicated by Δ and γ in FIG. 4. In other conventional receiver designs, an "automatic threshold" setting may be utilized which continuously adjusts to the received signal power level. However, this particular type of receiver is known to fail in the absence of both "1"s

and "0"s (or during long runs of either "1"s or "0"s).

The use of differential signaling in accordance with the present invention will essentially eliminate these problems, as shown in FIG. 5. In this case, the threshold TH of the receiver is set to provide equal channel current levels so that a differential DC level of zero is achieved. The transitions between logic "1" to logic "0" are therefore determined only by the zero crossings of the received signal. For the same three signal power levels L, S and H, it is shown in FIG. 5 that the zero-crossing is independent of the received signal power. Therefore, the recovered data signal from the differential receiver will be essentially independent of the strength of the received signal.

An exemplary transmitter circuit is illustrated in FIG. 6. The differential design exploits the inherent matching of devices 16 and 18, as discussed above, to provide equal emitted power, minimum noise injection. As shown, data signal D_i is applied as the input to amplifier 40, where amplifier 40 is configured to provide a pair of output signals of opposite value (referred to as non-inverting and inverting outputs). The non-inverting output is applied to the base of a first transistor 42, the collector of transistor 42 being grounded. The inverting output from amplifier 40 is applied as the input to the base of a second transistor 44, where the collector of transistor 44 is also grounded. The bases of transistors 42, 44 are coupled through resistors 46, 48 to a power supply rail 50. Emitters of transistors 42, 44 are coupled to LEDs 16 and 18, respectively, where LEDs 16, 18 are also coupled through resistors 52 to power supply rail 50. In operation, when data signal D_i is a logic "1", transistor 42 will be turned on and activate LED 16. Alternatively, when a logic "0" is present, the inverting output from amplifier 40 will go high and turn on transistor 44. In turn, the activation of transistor 44 will cause LED 18 to emit light.

An exemplary receiver 30, is illustrated in FIG. 7, in combination with photodiodes 26, 28. Receiver 30, contains a differential amplifier 62, where photodiode 26 is coupled to an inverting input of amplifier 62 and photodiode 28 is coupled to the noninverting input of amplifier 62. The complementary outputs from amplifier 62 are coupled to the inputs of a comparator 66. Since differential signaling is used, the DC level of the input to comparator 66 is maintained at a relative DC zero level, allowing the amplifiers to be directly connected to comparator 66 without any capacitive interconnection. Comparator 66 maintains a constant threshold TH, as discussed in association with FIG. 5, and provides the recovered data signal as a function of the input of the greatest magnitude.

Advantageously, the transmitter circuit of FIG. 6 may be replicated for each data channel and integrated as a single monolithic unit. Similarly, the receiver circuit of FIG. 7 may be replicated and integrated. The resultant array communication, when

used with an optical fiber ribbon cable, enjoys the maximum benefits of matching the optical and electrical characteristics of each data channel.

Claims

1. A data link array for providing communication between a plurality of transmitting devices and a plurality of receiving devices, CHARACTERIZED BY a differential array data link (10) including a plurality of 2N transmitting devices ($18_1-18_N; 20_1-20_N$) grouped in pairs such that a first device of each pair is activated to transmit a logic "0" and a second device of each pair is activated to transmit a logic "1", a plurality of 2N receiving devices ($26_1-26_N; 28_1-28_N$) grouped in pairs such that an output signal from a first device of each pair indicates the reception of a logic "0" and an output signal from a second device of each pair indicates the reception of a logic "1", and a plurality of 2N signal paths ($22_1-22_N; 24_1-24_N$) for coupling the plurality of 2N transmitting devices to the plurality of 2N receiving devices in a one-to-one manner, wherein the plurality of grouped pairs are defined as forming a plurality of N data channels.
2. An array as claimed in claim 1 wherein each data channel includes differential transmitting circuit means (16) responsive to an incoming data stream for providing an output to the first transmitting device for a logic "0" and an output to the second transmitting device for a logic "1", and differential receiving circuit means (30) coupled to the associated pair of receiving devices for providing an output data bit of logic "0" when the output from the first receiving device is greater than the output from the second receiving device and providing an output data bit of logic "1" when the output from the second receiving device is greater than the output from the first receiving device.
3. An array as claimed in claim 2 wherein the differential transmitting circuit means from each data channel are integrated to form a monolithic transmitting circuit.
4. An array data link as claimed in claim 2 or 3 wherein the differential receiving circuit means from each data channel are integrated to form a monolithic receiving circuit.
5. An array as claimed in any preceding claim wherein each of a plurality of the data channels includes multiplexing and demultiplexing means for transmitting a plurality of M separate data signals along that data channel.

6. An array as claimed in claim 5 wherein one data channel is reserved for the transmission of a frame clock so as to control the multiplexing and demultiplexing operations.
7. An array as claimed in any preceding claim wherein the plurality of 2N transmitting devices includes a plurality of 2N LEDs.
8. An array as claimed in any one of claims 1 to 6 wherein the plurality of 2N transmitting devices includes a plurality of 2N lasers.
9. An array as claimed in any preceding claim wherein the plurality of 2N receiving devices includes a plurality of 2N photodiodes.
10. An array as claimed in claim 7, 8 or 9 wherein the or each plurality of 2N devices is integrated to form a monolithic structure.
11. A bidirectional optical data link array for providing communication between a first plurality of devices and a second plurality of devices, **CHARACTERIZED BY** a differential array optical data link (100) including a first plurality of 2N semiconductor optical devices (e.g., 18₁-18_N; 20₁-20_N) grouped in pairs such that a first device of each pair is activated to communicate a logic "0" and a second device of each pair is activated to communicate a logic "1", a second plurality of 2N semiconductor optical devices (e.g., 18'₁-18'_N; 20'₁-20'_N) grouped in pairs such that a first device of each pair is activated to communicate a logic "0" and a second device of each pair is activated to communicate a logic "1", and a plurality of 2N signal paths (e.g., 22₁-22_N; 24₁-24_N) for coupling the first plurality of 2N semiconductor optical devices to the second plurality of 2N semiconductor optical devices in a one-to-one manner, the plurality of grouped pairs forming a plurality of N bidirectional data channels.
12. An array as claimed in claim 11 wherein each bidirectional data channel includes differential transmitting circuit means (16) coupled to the associated pair of devices of each plurality of 2N semiconductor optical devices for providing an output to the first device of said associated pair for a logic "0" and an output to the second device for a logic "1", and differential receiving circuit means (30) coupled to the associated pair of devices from each plurality of 2N semiconductor optical devices for providing an output data bit of logic "0" when the output from the first device is greater than the output from the second device and providing an output data bit of logic "1" when the output from the second device is greater than the output from the first device, a pair of co-located differential transmitting and receiving circuit means being disposed at each end of each data channel.
13. An array as claimed in claim 12 wherein for each data channel, the co-located differential transmitting and receiving circuit means are integrated to form a monolithic unit, there being a first plurality of N monolithic units associated with the first plurality of 2N semiconductor optical devices, and a second plurality of N monolithic units associated with the second plurality of 2N semiconductor optical devices.
14. An array as claimed in claim 13 wherein the first plurality of N monolithic units are integrated to form a single structure, and the second plurality of N monolithic units are integrated to form a single structure.
15. An array as claimed in claim 12, 13 or 14 including means for controlling the flow of data between the first plurality of 2N semiconductor optical devices and the second plurality of 2N semiconductor optical devices.
16. An array as claimed in claim 15 wherein the controlling means provides for the first plurality of 2N semiconductor optical devices to transmit and the second plurality of 2N semiconductor optical devices to receive during a first predetermined time period τ_1 , and for the second plurality of 2N semiconductor optical devices to transmit and the first plurality of 2N semiconductor optical devices to receive during a second predetermined time period τ_2 .
17. An array as claimed in claim 15 or 16 wherein the controlling means includes one data channel reserved for the transmission of a frame clock to control the transmission between the pluralities of 2N semiconductor optical devices.
18. An array as claimed in any one of claims 11 to 17 wherein the first and second pluralities of 2N semiconductor optical devices each include LEDs.
19. An array as claimed in any one of claims 11 to 17 wherein the first and second pluralities of 2N semiconductor optical devices each include a semiconductor laser.
20. An array as claimed in claim 18 or 19 wherein the first plurality of 2N semiconductor optical devices is integrated to form a first monolithic structure and the second plurality of 2N semiconductor

optical devices is integrated to form a second monolithic structure.

21. An array as claimed in any preceding claim wherein at least one signal path includes an optical fiber.

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22. An array as claimed in claim 21 wherein each signal path includes an optical fiber.

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23. An array as claimed in claim 22 wherein the plurality of 2N fiber signal paths include at least one fiber ribbon cable.

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FIG. 1

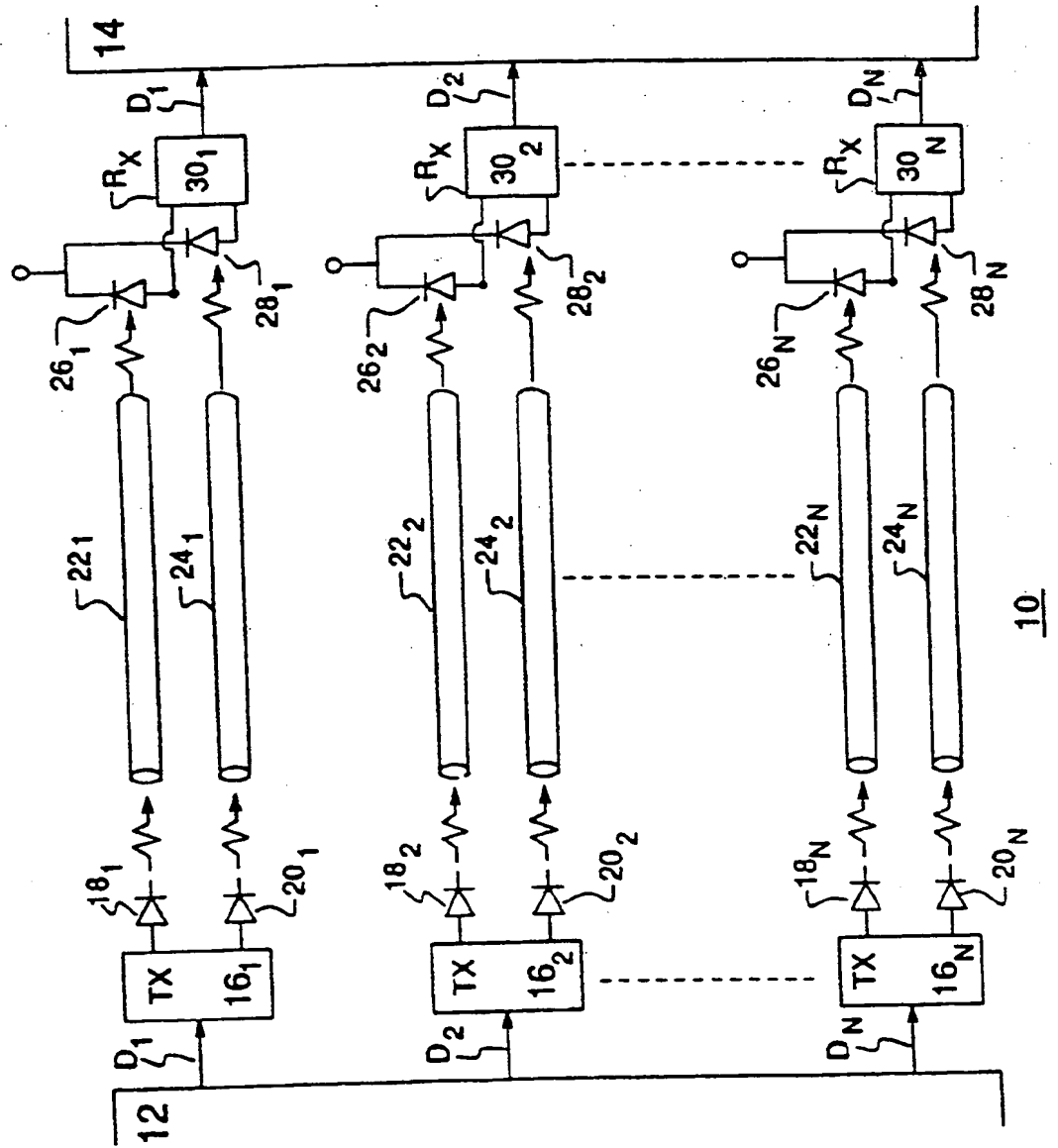


FIG. 2

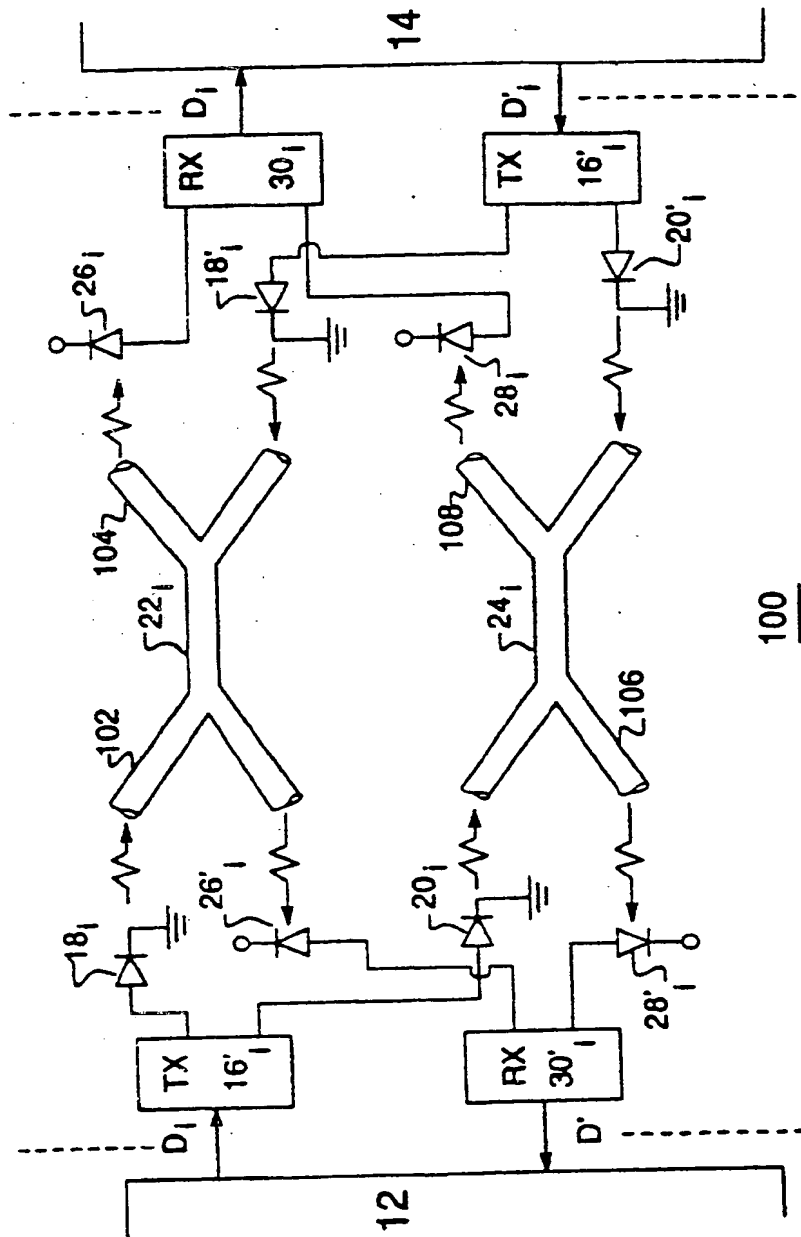


FIG. 3

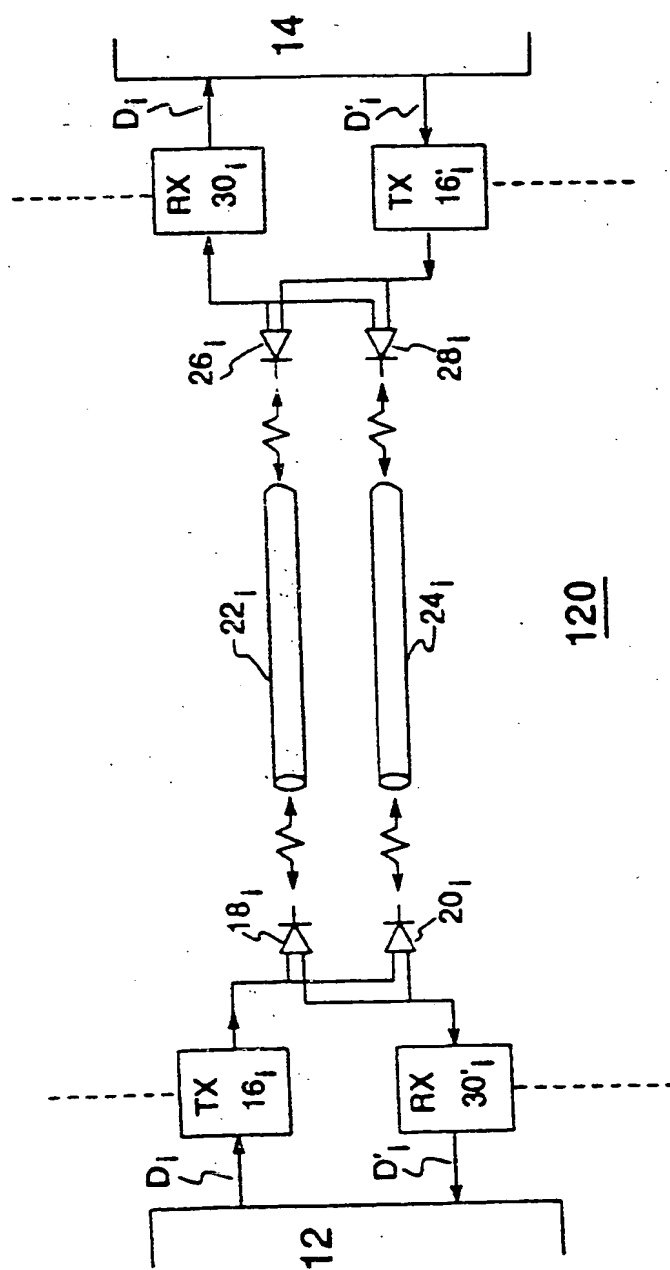


FIG. 5

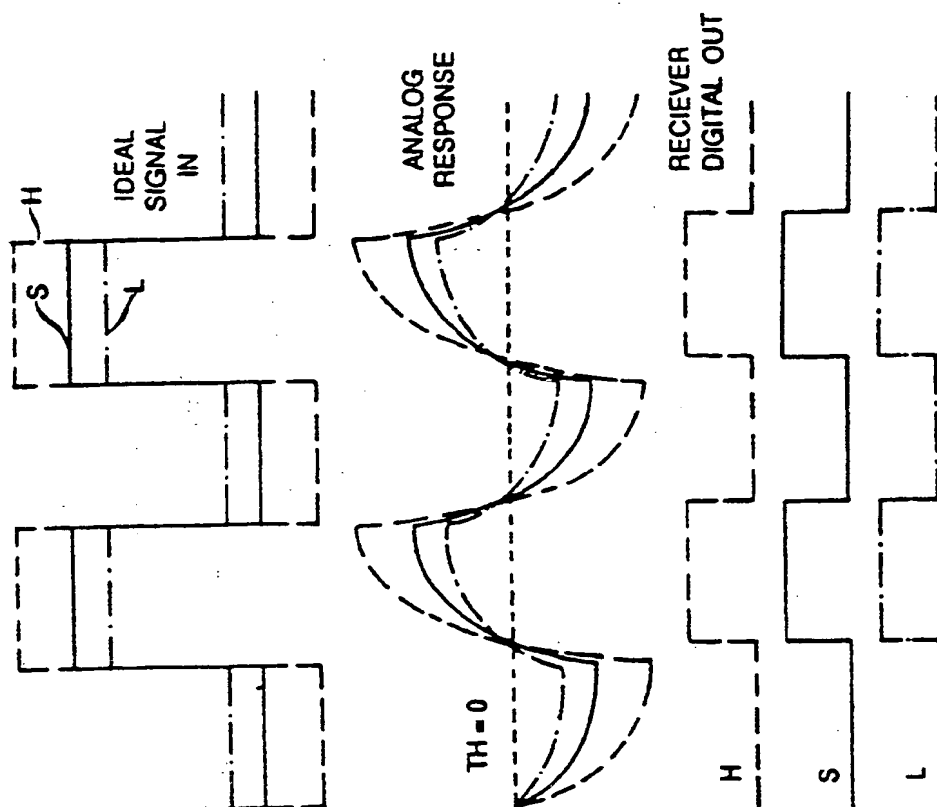


FIG. 4

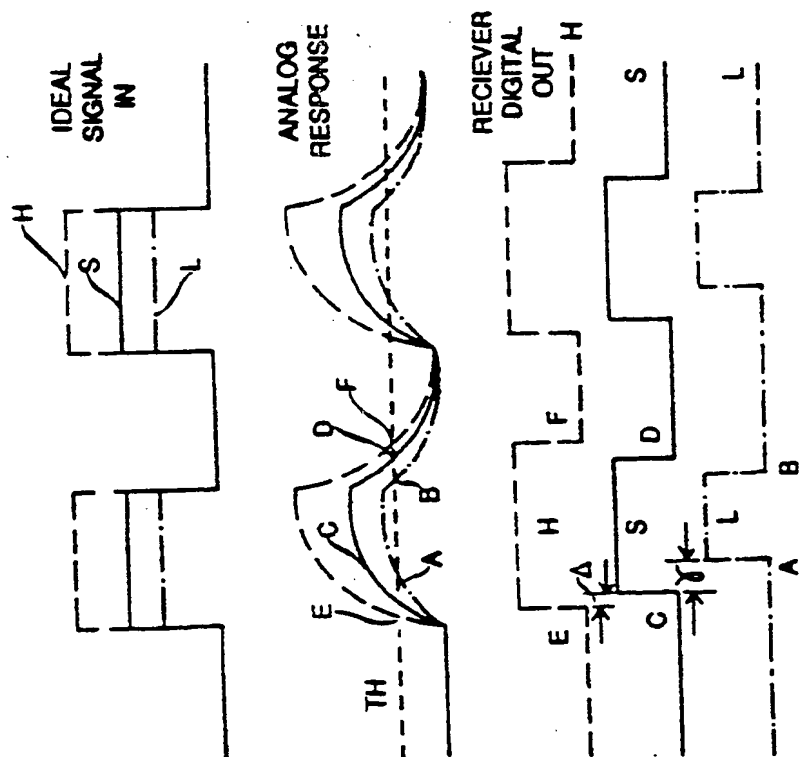


FIG. 6

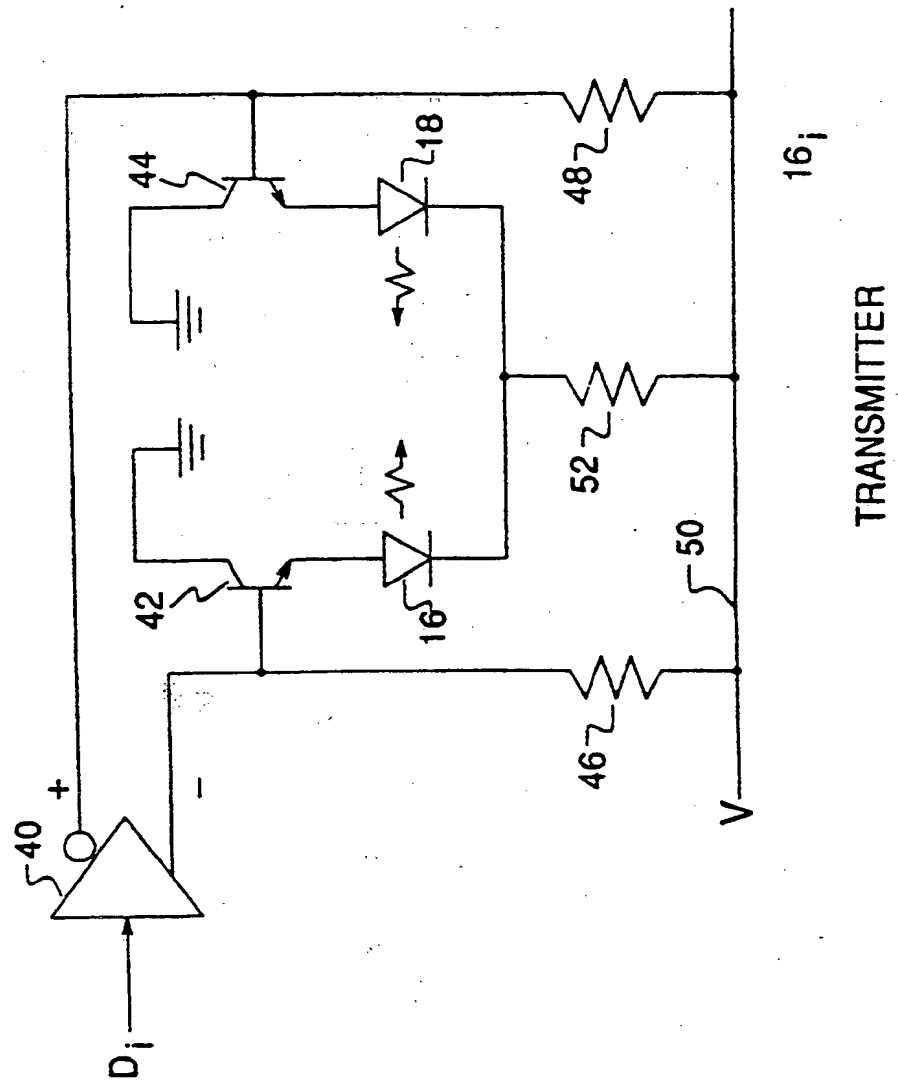


FIG. 7

